ABSTRACT

The present invention provides novel power saving methods for programmable logic array (PLA) circuits that includes diodes. One method is to store the results of a previous PLA operation, and bypass a new operation if the inputs are the same as previous operation. Another method is to reset the PLA outputs when the correct results can be achieved by resetting output latches. A large PLA is divided into smaller sub-PLA's while individual sub-PLA's are controlled separately. It is therefore possible to save power by bypassing unrelated sub-PLA's. PLA's of the present invention consume less power than equivalent prior art PLA's by orders of magnitudes. For most cases, PLA's of the present invention also have better performance and better cost efficiency. The design procedures are completely controlled by user-friendly computer aid design tools. The regular structures of PLA and the simplicity in connections allow us to avoid RC effects of conductor lines. We are able to achieve full performance improvement as IC technologies continue to progress into smaller and smaller critical dimensions.